

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A semiconductor memory comprising:

a plurality of memory mats each formed with a plurality of word lines, a plurality of bit lines, a spare bit line, and a plurality of memory cells, wherein, at a memory access, one of said plurality of memory mats is selected and one of said plurality of word lines in the selected memory mat is activated;

a plurality of bit line selection lines coupled to said plurality of memory mats, wherein respective ones of the plurality of bit lines in said plurality of memory mats are selected when one of said plurality of bit line selection lines is activated;

a spare bit line selection line coupled to said plurality of memory mats, wherein the respective spare bit lines in said plurality of memory mats are selected when said spare bit line selection line is activated; and

a pair of comparison circuits each formed with memory means and an output coupled to said spare bit line selection line, the memory means of one of said pair of comparison circuits being stored with a first defect information indicative of one of the bit line selection lines associated with a first defect and indicative of one of said plurality of memory mats associated with said first defect, the memory means of another of said pair of comparison circuits being stored with a second defect information indicative of one of the bit line selection lines associated with a second defect and indicative of one of said plurality of memory mats associated with said second defect, wherein each of said pair of comparison circuits compares the defect information with input signals including address signals indicative of selections of the memory mats and indicative of selections of the bit line selection lines.

2. (Original) The semiconductor memory according to claim 1, further comprising an OR circuit having inputs coupled to outputs of said pair of comparison circuits and an output coupled to said spare bit line selection line.

3. (Original) A semiconductor memory comprising:

a plurality of memory mats each formed with a plurality of word lines, a plurality of bit lines, a spare bit line, and a plurality of memory cells, wherein, at a memory access, one of said plurality of memory mats is selected and one of said plurality of word lines in the selected memory mat is activated;

a plurality of bit line selection lines coupled to said plurality of memory mats, wherein respective ones of the plurality of bit lines in said plurality of memory mats are selected when one of said plurality of bit line selection lines is activated;

a spare bit line selection line coupled to said plurality of memory mats, wherein the respective spare bit lines in said plurality of memory mats are selected when said spare bit line selection line is activated; and

a first comparison circuit and a second comparison circuit each formed with memory means and an output coupled to said spare bit line selection line, the memory means of said first comparison circuit being stored with a first defect information indicative of one of the bit line selection lines associated with a first defect and indicative of one of said plurality of memory mats associated with said first defect, the memory means of said second comparison circuit being stored with a second defect information indicative of one of the bit line selection lines associated with a second defect and indicative of one of said plurality of memory mats associated with said second defect, wherein said first comparison circuit compares the first defect information, and said second comparison circuit compares the second defect information, respectively with input signals including address

signals indicative of selections of the memory mats and indicative of selections of the bit line selection lines.

4. (Original) A semiconductor memory comprising:

a plurality of memory mats each formed with word lines, bit lines, a spare bit line, and memory cells, wherein, at a memory access, one of said memory mats is selected and one of said word lines in the selected memory mat is activated;

a plurality of bit line selection lines coupled to said memory mats, wherein respective ones of the bit lines in said plurality of memory mats are selected when one of said plurality of bit line selection lines is activated;

a spare bit line selection line coupled to said plurality of memory mats, wherein the respective spare bit lines in said plurality of memory mats are selected when said spare bit line selection line is activated; and

comparison means having an output coupled to said spare bit line selection line and formed with memory means stored with first and second defect information, wherein said first defect information is indicative of one of the bit line selection lines associated with a first defect and indicative of one of said plurality of memory mats associated with said first defect, wherein said second defect information is indicative of one of the bit line selection lines associated with a second defect and indicative of one of said plurality of memory mats associated with said second defect, wherein said comparison means compares said first and second defect information with address signals indicative of selections of the memory mats and indicative of selections of the bit line selection lines included in input signals supplied to the comparison means.

5. (Original) A semiconductor memory comprising:

a plurality of memory mats each formed with word lines, bit lines, a spare bit line, and memory cells, wherein, at a memory access, one of said memory mats is selected and one of said word lines in the selected memory mat is activated;

a plurality of bit line selection lines coupled to said memory mats, wherein respective ones of the bit lines in said plurality of memory mats are selected when one of said plurality of bit line selection lines is activated;

a spare bit line selection line coupled to said plurality of memory mats, wherein the respective spare bit lines in said plurality of memory mats are selected when said spare bit line selection line is activated; and

comparison means having an output coupled to said spare bit line selection line and formed with memory means stored with defect information indicative of ones of the bit line selection lines associated with defects and indicative of ones of said memory mats associated with the defects, respectively,

said comparison means being configured so as to compare said defect information with address signals indicative of selections of the memory mats and indicative of selections of the bit line selection lines included in input signals supplied to the comparison means wherein said spare bit line selection line is activated when the defect information agrees with said address signals.

6. (Original) A semiconductor memory comprising:

a plurality of memory mats each having a plurality of word lines, a plurality of bit lines, a spare bit line, and a plurality of memory cells, wherein, at a memory access, one of said plurality of memory mats is selected and one of said plurality of word lines is activated;

a plurality of bit line selection lines, each coupled to respective ones of the

plurality of bit lines of said plurality of memory mats;

a spare bit line selection line coupled to the spare bit lines of said plurality of memory mats; and

a comparison circuit having an output coupled to said spare bit line selection line, and memory means stored with a first information indicative of one of said plurality of bit line selection lines which is associated with a defect and a second information indicative of one of said plurality of memory mats which is associated with the defect, wherein said comparison circuit compares said first and second information with input signals including address signals indicative of one of said plurality of bit line selection lines and indicative of one of said plurality of memory mats.

7. (Original) A semiconductor memory comprising:

a plurality of memory mats, each having word lines, bit lines, a spare bit line, and memory cells, wherein, at a memory access, one of said plurality of memory mats is selected and one of said word lines is activated;

a plurality of bit line selection lines, each coupled to respective ones of the bit lines of said plurality of memory mats;

a spare bit line selection line coupled to the spare bit lines of said plurality of memory mats; and

redundancy control means coupled to said spare bit line selection line and formed with memory means and comparison means, said memory means being stored with a first information indicative of one of said plurality of bit line selection lines associated with a defect and a second information indicative of one of said plurality of memory mats associated with said defect, said comparison means comparing said first and second information with input signals including address

signals indicative of one of said plurality of bit line selection lines and indicative of one of said plurality of memory mats, wherein said spare bit line selection line is activated when said first and second information agrees with said address signals.

8. (Original) A semiconductor memory comprising:

a plurality of memory mats each having word lines, bit lines, a spare bit line, and memory cells, wherein, at a memory access, one of said plurality of memory mats is selected and one of said word lines is activated;

a plurality of bit line selection lines, each coupled to respective ones of the plurality of bit lines of said plurality of memory mats;

redundancy control means formed with memory means and comparison means, said memory means being stored with first information indicative of one of said plurality of bit line selection lines associated with a defect and second information indicative of one of said plurality of memory mats associated with said defect, said comparison means being configured so as to compare said first and second information with input signals including address signals indicative of one of said plurality of bit line selection lines and indicative of one of said plurality of memory mats; and

a spare bit line selection line coupled to the spare bit lines of said plurality of memory mats, supplied with an output of said redundancy control means and configured so as to be activated in response to the output of said redundancy control means when said first and second information agrees with said address signals.

9. (Original) A semiconductor memory comprising:

a plurality of memory mats each having word lines, bit lines, a spare bit line, and memory cells, wherein, at a memory access, one of said plurality of memory mats is selected and one of said word lines is activated;

a plurality of bit line selection lines, each coupled to respective ones of the plurality of bit lines of said plurality of memory mats;

a spare bit line selection line coupled to the spare bit lines of said plurality of memory mats; and

redundancy control means formed with:

memory means stored with defect information indicative of one of said plurality of bit line selection lines associated with a defect as well as one of said plurality of memory mats associated with the defect;

comparison means supplied with address signals indicative of said plurality of bit line selection lines as well as indicative of said plurality of memory mats and configured so as to compare said defect information with the supplied address signals; and

an output node coupled to said spare bit line selection line wherein said spare bit line selection line is activated in response to a comparison result of said comparison means when ones of the address signals agree with said defect information.

10. (Original) A semiconductor memory comprising:

a plurality of memory mats each having a plurality of word lines, a plurality of bit lines, a spare bit line, and a plurality of memory cells, wherein, at a memory access, one of said plurality of memory mats is selected and one of said plurality of word lines of the selected memory mat is activated;

a plurality of bit line selection lines each coupled to ones of the plurality of bit lines of said plurality of memory mats;

a spare bit line selection line coupled to the spare bit lines of said plurality of memory mats; and

a redundancy circuit having an output coupled to said spare bit line selection line and programmed to respond to a first defect mode associated with a defect in one of said plurality of memory mats so as to activate said spare bit line selection line depending on an access to said one of said plurality of memory mats and to respond to a second defect mode associated with a defect related to one of said plurality of bit line selection lines so as to activate said spare bit line selection line depending on an access of any one of said plurality of memory mats.

11. (Original) A semiconductor memory comprising:

a plurality of memory mats each having word lines, bit lines, a spare bit line, and memory cells, wherein, at a memory access, one of said plurality of memory mats is selected and one of said word lines of the selected memory mat is activated;

a plurality of bit line selection lines each coupled to ones of the bit lines of said plurality of memory mats;

a spare bit line selection line coupled to the spare bit lines of said plurality of memory mats; and

redundancy control means having an output coupled to said spare bit line selection line and programmed so as to activate said spare bit line selection line in response to a first defect mode associated with a defect in one of said plurality of memory mats depending upon an access to said one of said plurality of memory mats and in response to a second defect mode associated with a defect related to one of said plurality of bit line selection lines depending upon an access of any one

of said plurality of memory mats.

Claims 12-21. (Canceled)